

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	23	(trac\$3 and clock\$2 and tim\$3 and emulat\$3).clm.	US-PGPUB	OR	OFF	2006/02/03 17:54
L3	30	(trac\$3 and clock\$2 and emulat\$3).clm.	US-PGPUB	OR	OFF	2006/02/03 17:54

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L1	434	714/45.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/03 15:18
L3	433	processor and trace and clock and timing and stall\$2 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/03 17:04
L6	20	swoboda.in. and texas.as. and @ad<"20010901" and @ad>"20000830"	USPAT	OR	OFF	2006/02/03 17:08
S1	202	703/28.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/03 12:43
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» Key

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IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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Performance Evaluation of the Memory Hierarchy of a Desktop PC using Commodity Chips with Specific ...

A Pavlov, JL Béchenec, D Etienne - EUROMICRO 97.'New Frontiers of Information Technology', ..., 1997 - doi.ieeecs.org

... The final specific **trace** is got by dis- carding all the ... to the external memory (the

wall **clock** time which ... The **timing** aspect of the final specific **trace** is thus ...

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Latent Design Faults in the Development of the Multiflow TRACE/200

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... To make this easier, we varied **timing**, voltage, and ... The system **clock** generator could

switch between a fast ... The basic philosophy of the **TRACE** VLIW calls for ...

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Verification Methodology of Compatible Microprocessors

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large **trace** file ... mix, FSM transition coverage, pipeline **stall** event coverage ...

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... In spite of the **clock** cycle disparities, the **TRACE** 14/200 yields approximately

4-10 times the performance of a VAX that costs twice as much, and from 1/2 to 1 ...

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M Forsyth, S Mangelsdorf, E Delano, C Gleason, J ... - Proceedings of COMPCON, 1991 - ieeexplore.ieee.org

... External PC board **trace** delays are used to control placement of **clock** edges and

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... that the characteristics of an application **trace** that track ... qualify the **clock** can

potentially introduce **timing** critical skews ... when few blocks can be **clock** gated ...

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... relevant data from the standard **trace** for different ... are abstracted from their individual

timing informa- tion ... and some parameters for the **clock** generation path ...

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High-performance CMOS system design using wave pipelining

KJ Nowka - 1995 - reports.stanford.edu

... additional tran- sistors within the pipeline to provide **stall** capabilities are ... The

clock timing constraints which must be met for correct circuit operation in ...

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Clock rate versus IPC: The end of the road for conventional microarchitectures

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... of our analytical models as in- puts to SimpleScalar-based **timing** simulation, we ...

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Simulating Asynchronous Architectures on Transputer Networks

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... One solution to **clock-related timing** problems is to ... The absence of one parallelity event from a pair in the final **trace** indicates the oc- currence of a ...

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